

JMTG035N04L

Features

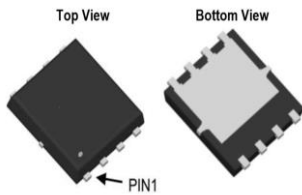
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- 100% UIS Tested
- 100% V_{DS} Tested
- Halogen-free; RoHS-compliant

Applications

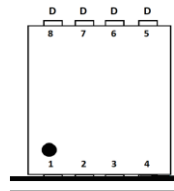
- Load Switch
- PWM Application
- Power Management

Product Summary

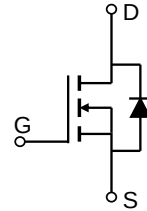
Parameters	Value	Unit
V_{DSS}	40	V
$V_{GS(th_Typ)}$	1.5	V
$I_D(@V_{GS}=10V)$	100	A
$R_{DS(ON_Typ)}(@V_{GS}=10V)$	2.4	mΩ
$R_{DS(ON_Typ)}(@V_{GS}=4.5V)$	3.0	mΩ



PDFN5X6-8L



Pin Assignment



Schematic Diagram

Ordering Information

Device	Marking	MSL	Form	Package	Reel(pcs)	Per Carton (pcs)
JMTG035N04L	G035N04L	1	Tape&Reel	PDFN5x6-8L	5000	50000

Absolute Maximum Ratings (@ $T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-to-Source Voltage	40	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D	Continuous Drain Current	$T_C = 25^\circ\text{C}$ $T_C = 100^\circ\text{C}$	$\begin{matrix} 100 \\ 63 \end{matrix}$ A
I_{DM}	Pulsed Drain Current ⁽¹⁾	Refer to Fig.4	A
E_{AS}	Single Pulsed Avalanche Energy ⁽²⁾	306	mJ
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$ $T_C = 100^\circ\text{C}$	$\begin{matrix} 125 \\ 50 \end{matrix}$ W
T_J, T_{STG}	Junction & Storage Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Max	Unit
R	Thermal Resistance, Junction to Ambient ⁽³⁾	37	$^\circ\text{C/W}$
R	Thermal Resistance, Junction to Case	1.0	

Electrical Characteristics (T_J = 25°C unless otherwise specified)

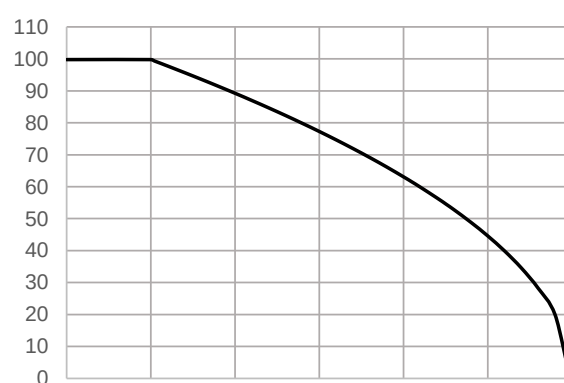
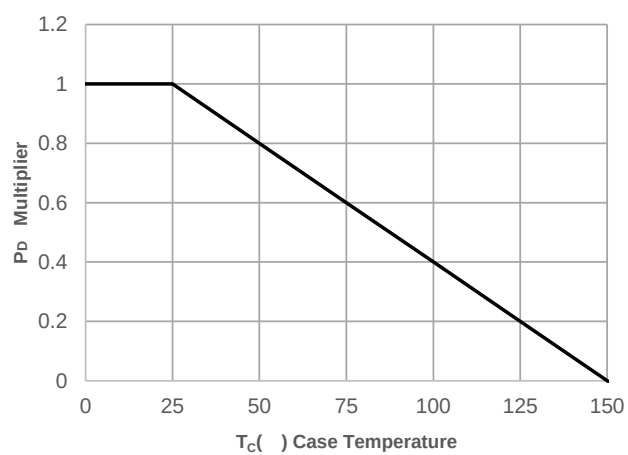
Ubln M57TQ4C /P 4TJ22300.794.76 reW*nBT3>BDC 25.92 671.5 543.36 14.76 reW3*nBT4 8.76 TTyp.0 1 428.26x723.22 Unit g0 G(T)8(y)3E

Off Characteristics

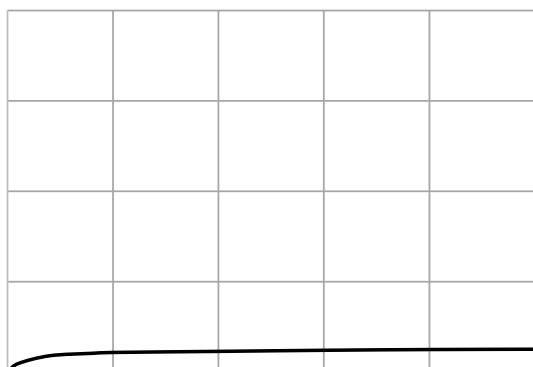
V _{(BR)DSS}	40	-	-	V
I _{DSS}	-	-	1.0	μA
I _{GSS}	-	-	±100	V nA
V _{GS(th)G[V]]TJETQq25.83.nBT/F4 9.8a7.762BT/F4 9.72 Tf1 0 0 1 528.84 66 nBT/F2 8.76 Tf1 0 0 1 389.4 632.71 Tm0 g0 G[V]]TJETQq25.92 627.320.6323.36ZETQq25.83.n}				

Typical Performance Characteristics

Figure 1: Power De-rating



Typical Performance Characteristics



Typical Performance Characteristics

Figure 11: Normalized Breakdown voltage vs. Junction Temperature

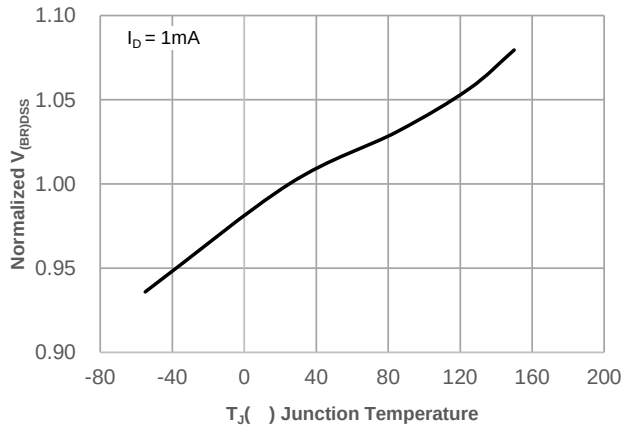


Figure 12: Normalized on Resistance vs. Junction Temperature

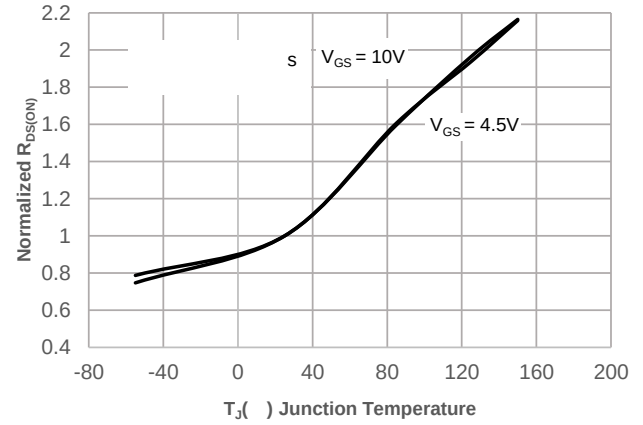


Figure 14: $R_{DS(ON)}$ vs. V_{GS}

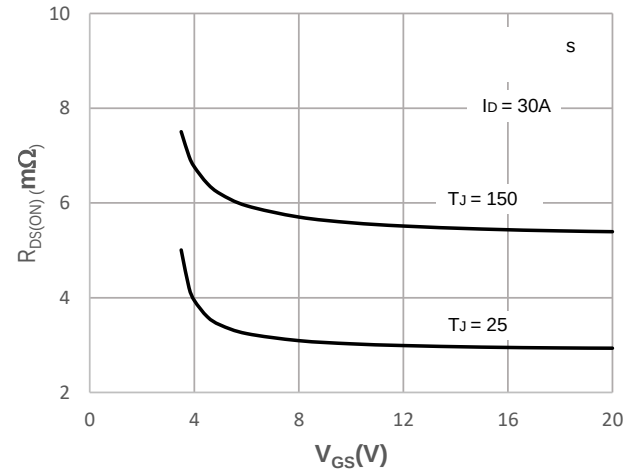
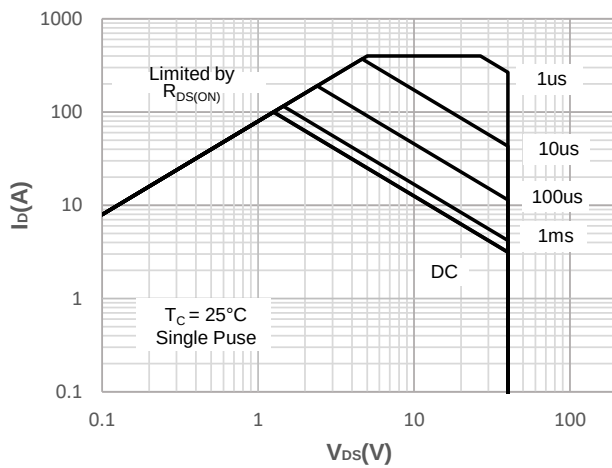


Figure 15: Maximum Safe Operating Area



Test Circuit

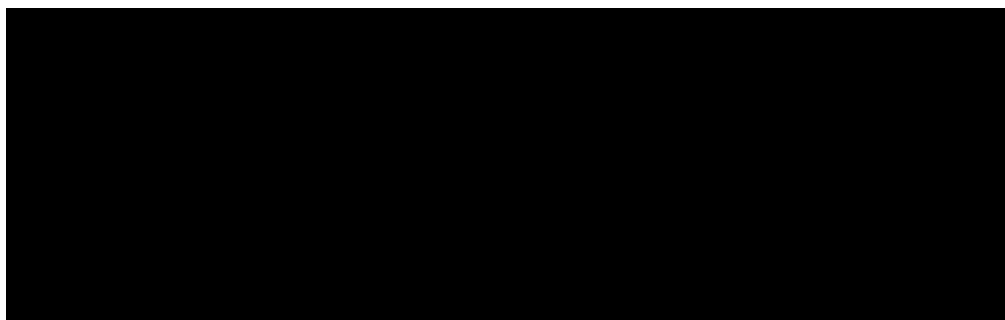


Figure 1: Gate Charge Test Circuit & Waveform

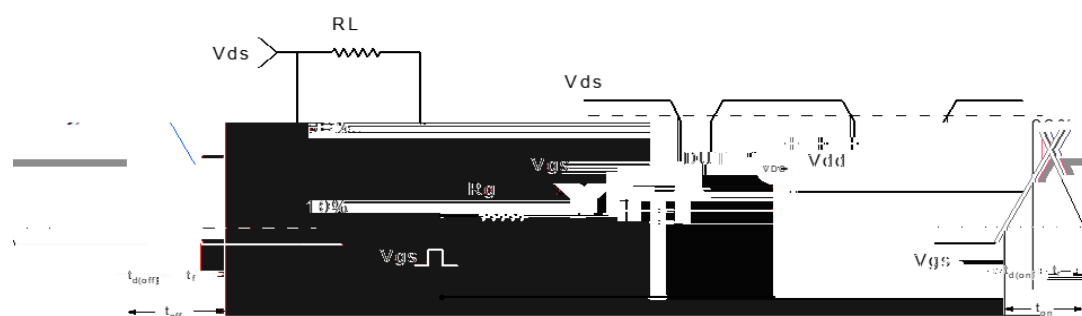
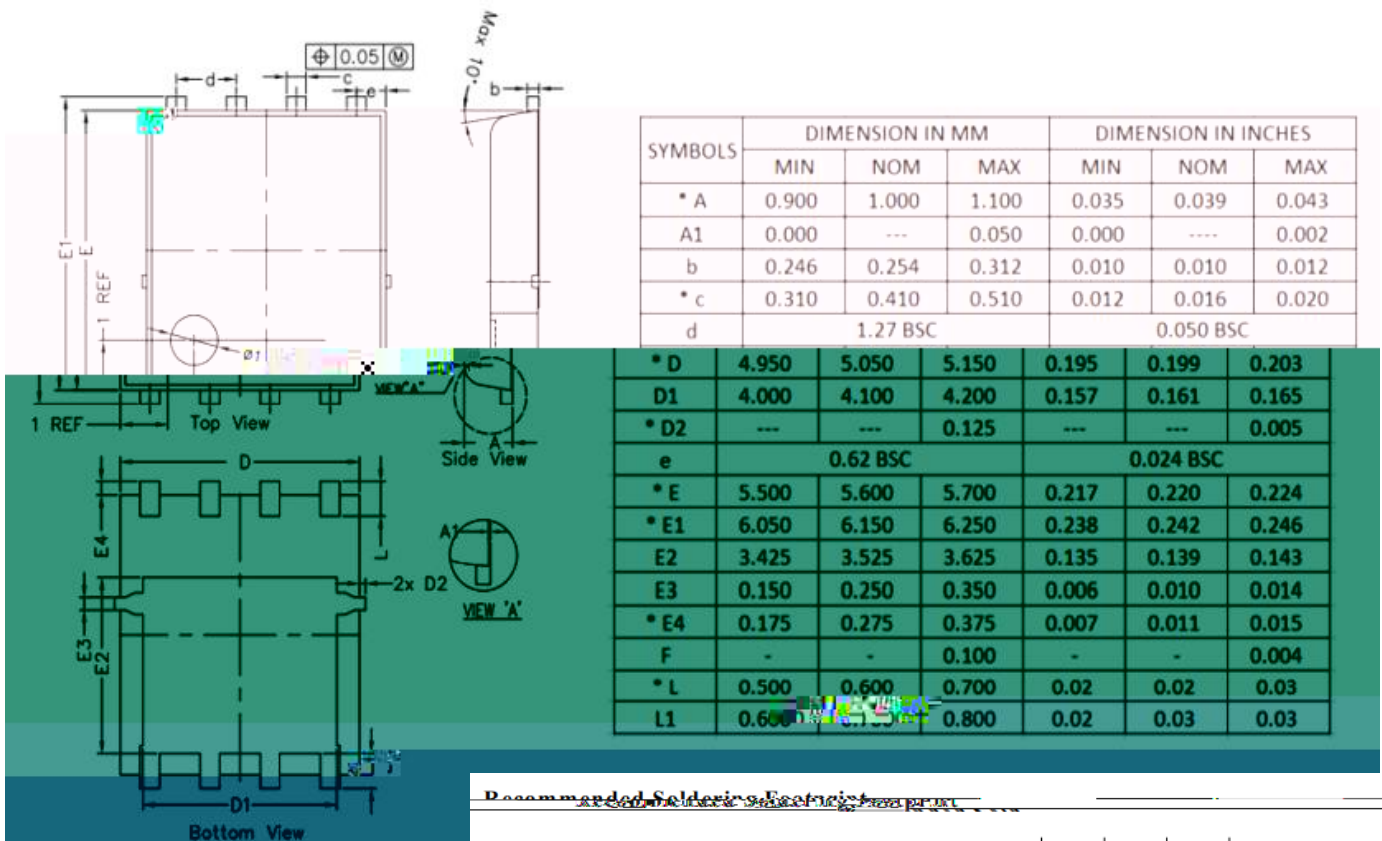
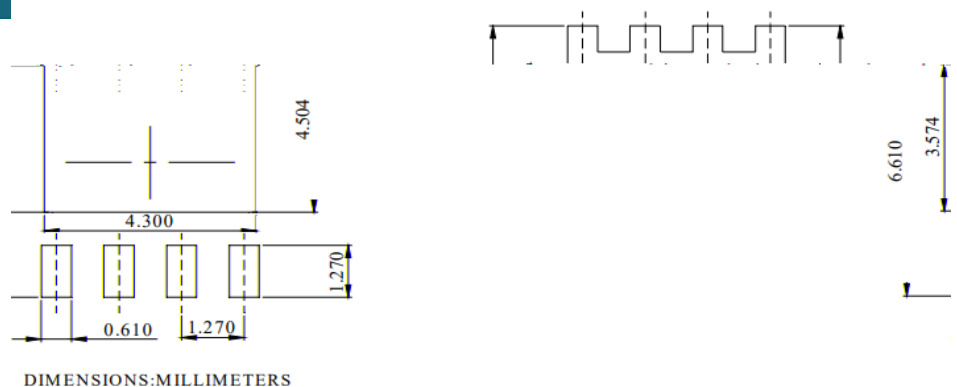


Figure 2: Resistive Switching Test Circuit & Waveform

Package Mechanical Data(PDFN 5X6-8L)



Recommended Soldering Footprint



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