

JMTQ080P03A

Features

- Excellent $R_{DS(ON)}$ and Low Gate Charge
- 100% UIS Tested
- 100% V_{DS} Tested
- Halogen-free; RoHS-compliant
- Pb-free plating

Applications

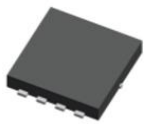
- Load Switch
- PWM Application
- Power Management

Product Summary

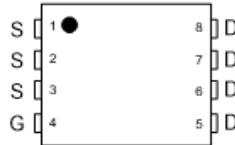
Parameters	Value	Unit
V_{DS}	-30	V
$V_{GS(th)}_{Typ}$	-1.5	V
$I_D(@V_{GS}=-10V)$	-50	A
$R_{DS(ON)}_{Typ}(@V_{GS}=-10V)$	5.9	mΩ
$R_{DS(ON)}_{Typ}(@V_{GS}=-4.5V)$	8.1	mΩ



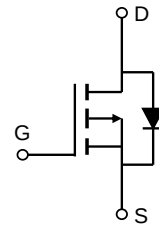
Top View



Bottom View



Pin Assignment



Schematic

PDFN3X3-8L

Ordering Information

Device	Marking	MSL	Form	Package	Reel(pcs)	Per Carton (pcs)
JMTQ080P03A	Q080P03A	1	Tape&Reel	PDFN3x3-8L	5000	50000

Absolute Maximum Ratings (@ $T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-to-Source Voltage	-30	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D	Continuous Drain Current	$T_C = 25^\circ\text{C}$ $T_C = 100^\circ\text{C}$	A
I_{DM}	Pulsed Drain Current ⁽¹⁾	Refer to Fig.4	A
E_{AS}	Single Pulsed Avalanche Energy ⁽²⁾	133	mJ
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$ $T_C = 100^\circ\text{C}$	W
T_J, T_{STG}	Junction & Storage Temperature Range	-55 to 150	$^\circ\text{C}$

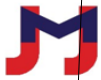
Thermal Characteristics

Symbol	Parameter	Max	Unit
R	Thermal Resistance, Junction to Ambient ⁽³⁾	41	$^\circ\text{C/W}$
R	Thermal Resistance, Junction to Case	4.2	$^\circ\text{C/W}$

Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	I _D = -250μA, V _{GS} = 0V	-30	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -30V, V _{GS} = 0V	-	-	-1.0	μA
I _{GSS}	Gate-Body Leakage Current	V _{DS} = 0V, V _{GS} = ±20V	-	-	±100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = -250μA	-1.1	-1.5	-2.0	V
R _{DS(ON)}	Static Drain-Source ON-Resistance ⁽⁴⁾	V _{GS} = -10V, I _D = -20A	-	5.9	7.4	mΩ
		V _{GS} = -4.5V, I _D = -10A	-	8.1	10.1	mΩ
Dynamic Characteristics						
R _g	Gate Resistance	f = 1MHz	-	11.5	-	Ω
C _{iss}	Input Capacitance	V _{GS} = 0V, V _{DS} = -15V, f = 1MHz	2405	3366	4545	pF
C _{oss}	Output Capacitance		336	471	635	pF
C _{rss}	Reverse Transfer Capacitance		232	324	438	pF
Q _g	Total Gate Charge	V _{GS} = 0 to -10V V _{DS} = -15V, I _D = -10A	-	59	-	nC
Q _{gs}	Gate Source Charge		-	9.5	-	nC
Q _{gd}	Gate Drain("Miller") Charge		-	14	-	nC
Switching Characteristics						
t _{d(on)}	Turn-On DelayTime	V _{GS} = -10V, V _{DD} = -15V I _D = -10A, R _{GEN} = 2.7Ω	-	6.8	-	ns
t _r	Turn-On Rise Time		-	5.7	-	ns
t _{d(off)}	Turn-Off DelayTime		-	112	-	ns
t _f	Turn-Off Fall Time		-	78	-	ns
Body Diode Characteristics						
I _S	Maximum Continuous Body Diode Forward Current		-	-	-50	A
I _{SM}	Maximum Pulsed Body Diode Forward Current		-	-	-202	A
V _{SD}	Body Diode Forward Voltage	V _{GS} = 0V, I _S = -20A	-		-1.2	V
trr	Body Diode Reverse Recovery Time	I _F = -10A, di/dt = 100A/us	15	21	29	ns
Qrr	Body Diode Reverse Recovery Charge		-	9.8	-	nC

- Notes:
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
 2. E_{AS} condition: Starting $T_J = 25^\circ\text{C}$, $V_{DD} = -15\text{V}$, $V_{GS} = -10\text{V}$, $R_G = 25\Omega$, $L = 0.5\text{mH}$, $I_{AS} = -23.1\text{A}$, $V_{DD} = 0\text{V}$ during time in avalanche.
 3. R is measured with the device mounted on a 1inch^2 pad of 2oz copper FR4 PCB.
 4. Pulse Test: Pulse Width $\leq$ $\leq 0.5\%$.



Typical Performance Characteristics

Figure 1: Power De-rating

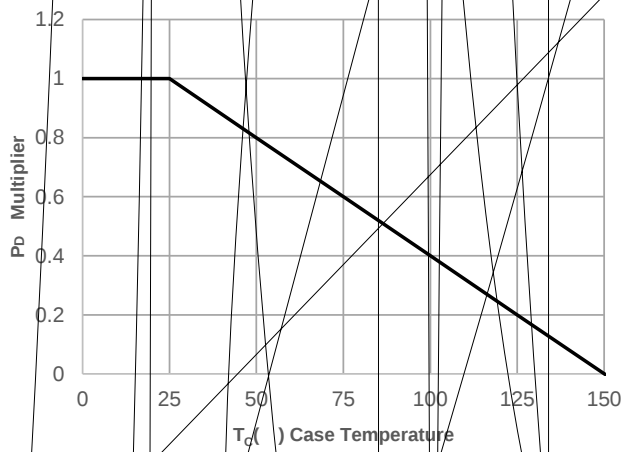
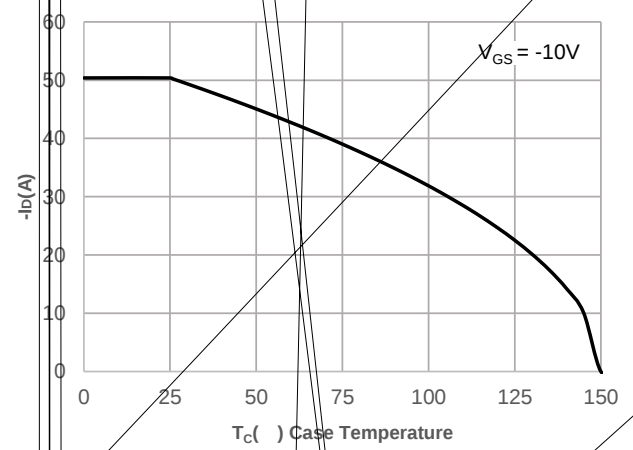
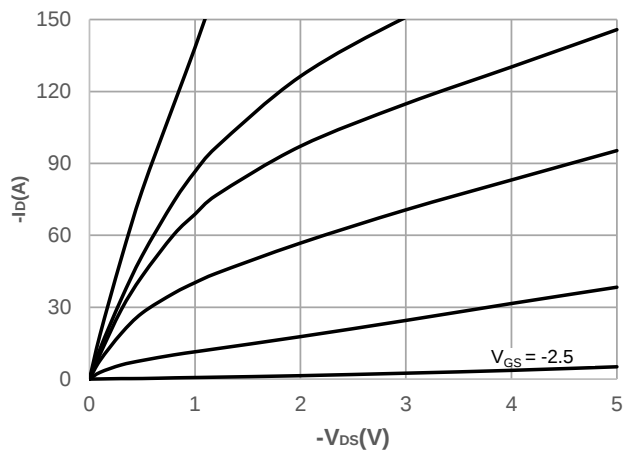


Figure 2: Current De-rating



Typical Performance Characteristics

Figure 5: Output Characteristics



Typical Performance Characteristics

Figure 11: Normalized Breakdown voltage vs. Junction Temperature

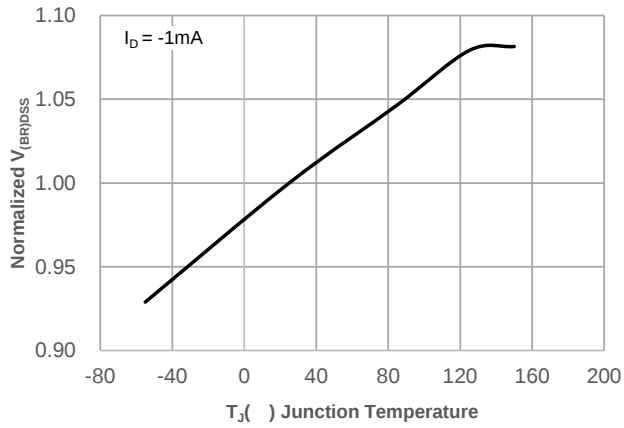


Figure 12: Normalized on Resistance vs. Junction Temperature

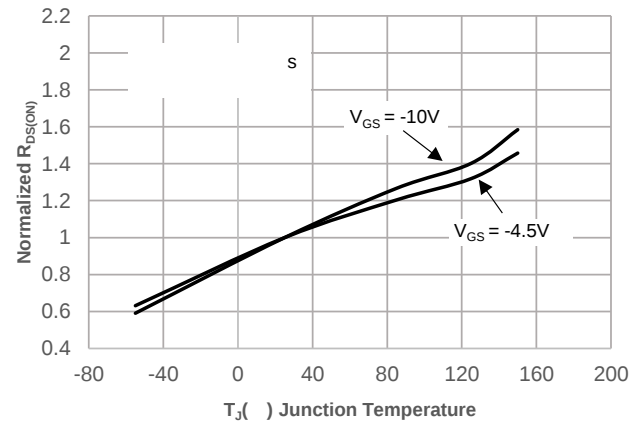


Figure 13: Normalized Threshold Voltage vs. Junction Temperature

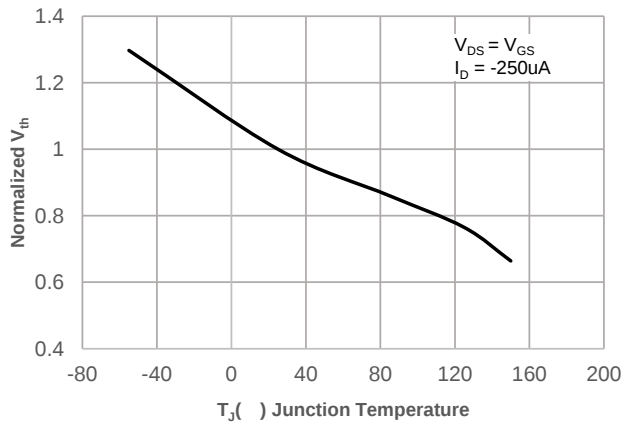


Figure 14: $R_{DS(ON)}$ vs. V_{GS}

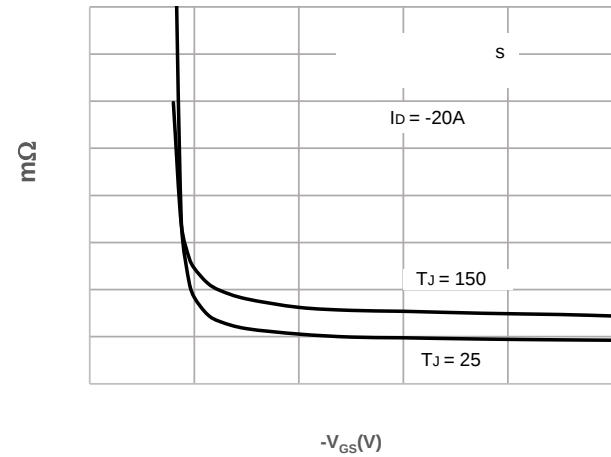
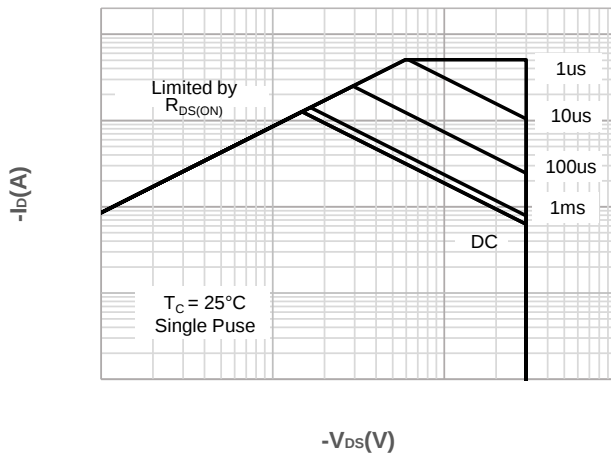


Figure 15: Maximum Safe Operating Area



Test Circuit

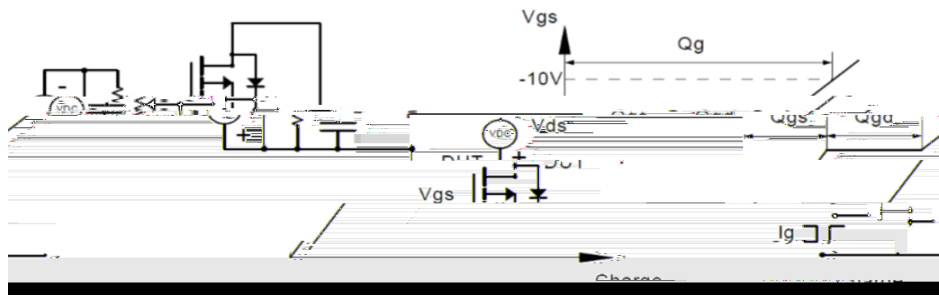


Figure 1: Gate Charge Test Circuit & Waveform

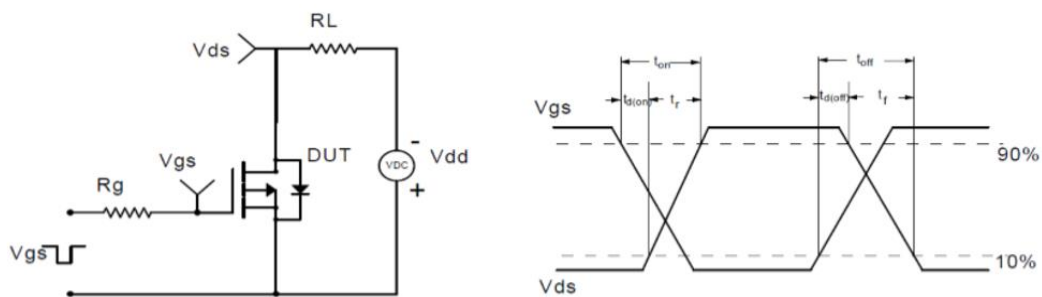


Figure 2: Resistive Switching Test Circuit & Waveform

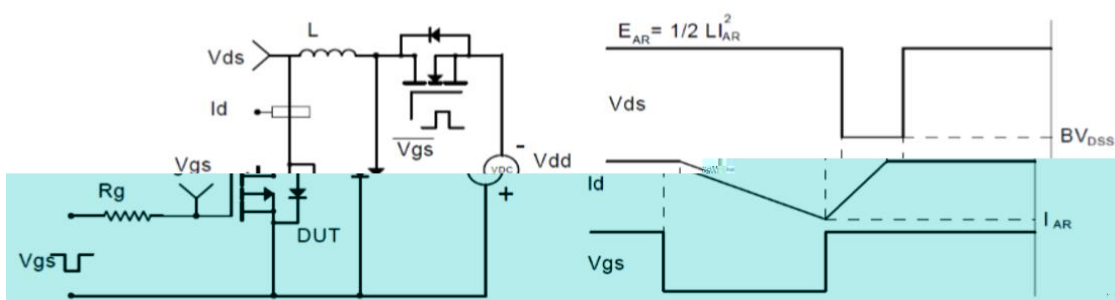
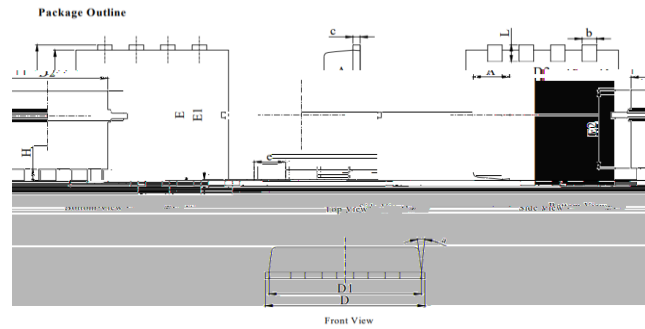


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform



Figure 4: Diode Recovery Test Circuit & Waveform

Package Mechanical Data(PDFN3x3-8L)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. ALL DIMENSIONS IN MILLIMETER (ANGLE IN DEGREE).

Q-M	MIN	NOM.	MAX
A	0.70	0.75	0.80
B	0.25	0.30	0.35
C	0.10	0.20	0.25
D	3.00	3.15	3.25
D1	2.95	3.05	3.15
D2	2.39	2.49	2.59
E	0.20	0.25	0.30
F	0.20	0.25	0.30
G	0.20	0.25	0.30
H	0.20	0.25	0.30
I	0.20	0.25	0.30
J	0.20	0.25	0.30
K	0.20	0.25	0.30
L	0.20	0.25	0.30
M	0.20	0.25	0.30
N	0.20	0.25	0.30
O	0.20	0.25	0.30
P	0.20	0.25	0.30
Q	0.20	0.25	0.30
R	0.20	0.25	0.30
S	0.20	0.25	0.30
T	0.20	0.25	0.30
U	0.20	0.25	0.30
V	0.20	0.25	0.30
W	0.20	0.25	0.30
X	0.20	0.25	0.30
Y	0.20	0.25	0.30
Z	0.20	0.25	0.30

Recommended Soldering Footprint



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